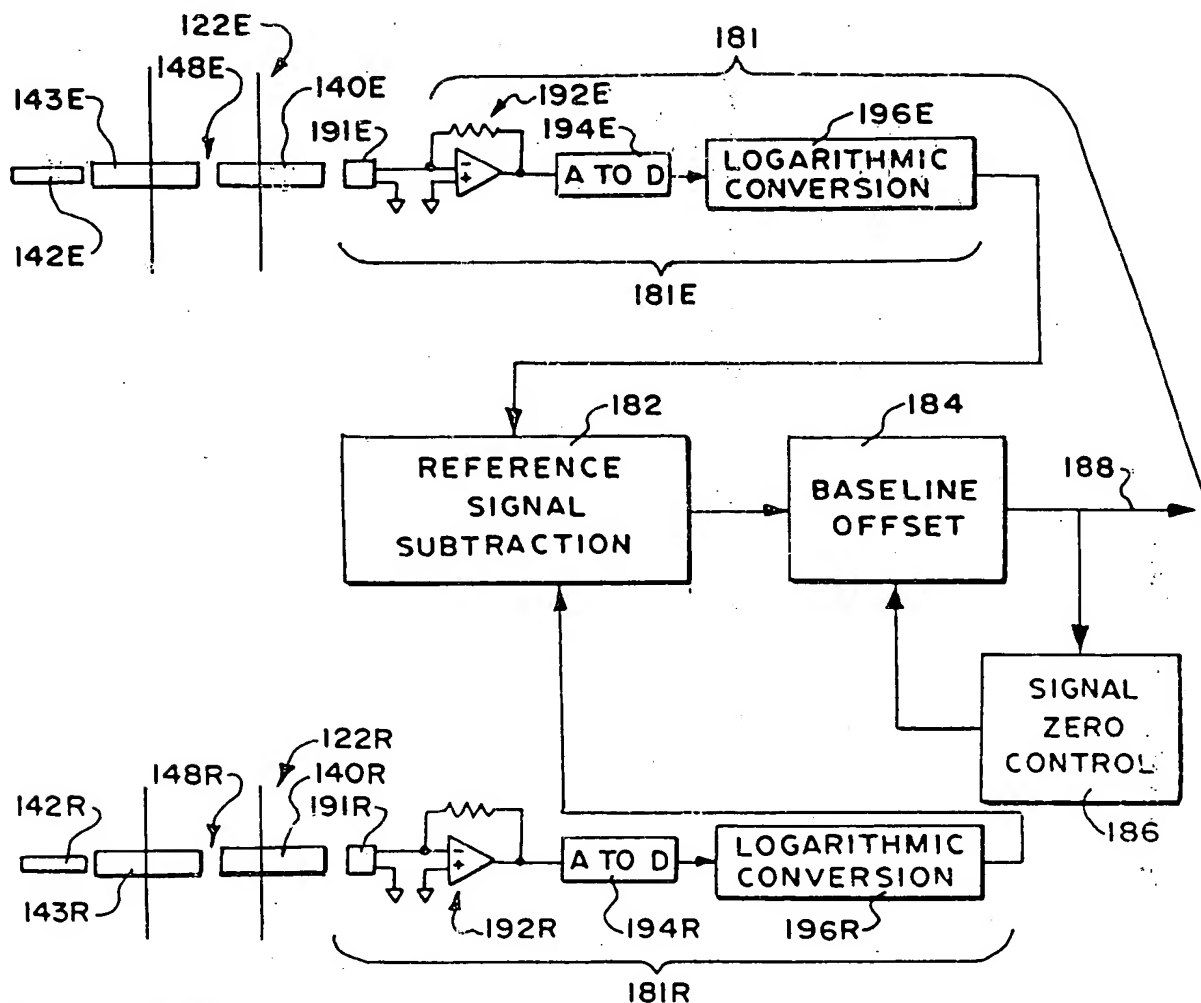
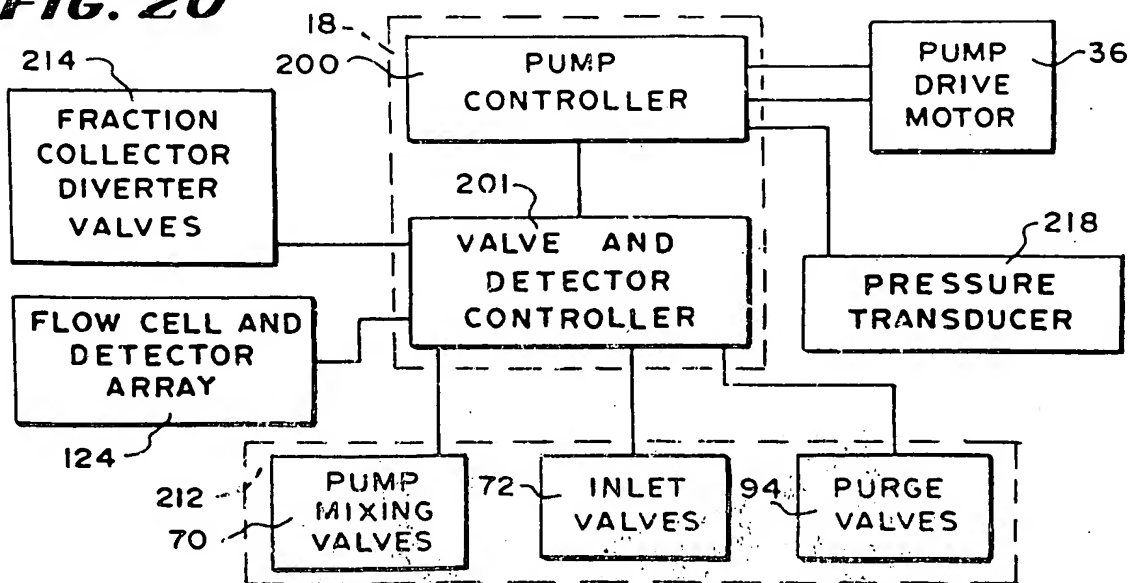


**FIG. 19**



**FIG. 20**



The diagram illustrates a signal processing system with two parallel channels, labeled 'E' (top) and 'R' (bottom). Each channel consists of a series of input blocks (142E, 143E, 148E, 140E for channel E; 142R, 143R, 148R, 140R for channel R) followed by a complex circuit (192E, 192R) containing resistors, capacitors, and operational amplifiers. The outputs of these circuits are fed into A/D converters (194E, 194R) and then into logarithmic conversion blocks (196E, 196R). The outputs of the logarithmic conversion blocks are fed into a reference signal subtraction block (182) and a baseline offset block (184). The baseline offset block also receives input from a signal zero control block (186). The final outputs of the system are labeled 188 and 186.